EclaireXL - Feature #65

Implement ATA to SPI bridge

05/24/2018 08:44 PM - foft

Status:	New	Start date:	05/24/2018
Priority:	Normal	**Due date:**	
Assignee:		**% Done:**	0%
Category:		**Estimated time:**	0:00 hour
Target version:			

Description

There is plenty of software for the Atari which accesses ATA hard drives via a simple register interface. Find out what this interface is and wire it up to the SD card directly. So its possible to use it like the compact flash in an incognito for instance.

History

#1 - 05/24/2018 08:52 PM - sadosp

foft wrote:

> There is plenty of software for the Atari which accesses ATA hard drives via a simple register interface. Find out what this interface is and wire it up to the SD card directly. So its possible to use it like the compact flash in an incognito for instance.

P-o-ss-i-b-i-l-i-t-i-e-s :-)

#2 - 05/25/2018 06:30 AM - foft

I need to prepare a document outlining the minimum requirements of IDE emulation since I'm explaining the same thing in multiple locations at the moment. ;) Absolute minimum requirement is the 8 basic IDE registers, and it's useful to be able to reset the device. These are the SIDE2 registers as an example:

```
IDE_DATA    equ $D5f0
IDE_ERR     equ $D5f1
IDE_SCNT    equ $D5f2
IDE_SNUM    equ $D5f3        ; LBA 0
IDE_CYLL    equ $D5f4        ; LBA 1
IDE_CYLH    equ $D5f5        ; LBA 2
IDE_HEAD    equ $D5f6        ; LBA 3 ($Ex)
IDE_STAT    equ $D5f7
IDE_CTRL    equ $D5f8        ; Device control (used for device reset)
```

One could implement a latched sixteen bit data register to do away with the need for 8-bit PIO mode, but I'm not sure off the top of my head how that would work with the PDM Player (since I didn't code up an IDE Plus 2.0 version yet).

Bare minimum required commands are read (0x20), write (0x30), Indentify device (0xEC) and Set Features (0xEF, if no sixteen bit data bus is provided). Only the following information from the Identify Device buffer is employed by APT tools:
1   Number of logical cylinders
3   Number of logical heads
5   Number of logical sectors per track
10-19   Serial number (20 ASCII characters)
23-26   Firware revision (8 ASCII characters)
27-46   Model number (40 ASCII characters)
60-61   Total number of user addressable sectors (LBA mode only)
CHS data is used by the partition editor when laying out the MBR. The three strings can be populated with generic place-holder information if necessary.

Of course I'm not delving into the entire APT implementation here, which ideally requires a PBI device ROM.

#3 - 05/25/2018 06:31 AM - foft

Above was info from flashjazzcat on the forum

#4 - 06/11/2018 08:40 PM - foft

Some links..
https://www.pjrc.com/tech/8051/ide/wesley.html#idereg
http://atariage.com/forums/topic/279232-fujiconvert-01/page-3

Simple read seems to be:
sector address-> 4 lba regs with $e0 in high part

scnt-> 1
stat-> cmd
data-> read each byte at a time

#5 - 06/11/2018 08:53 PM - foft

https://wiki.osdev.org/ATA_PIO_Mode

Probably want at least DRQ, RDY and BSY in the status reg

#6 - 06/11/2018 09:04 PM - foft

Identify:0xec
0->SCNT,SNUM,CYLL,CYLH
0xa0->HEAD
0xec >STAT
read stat -> if 0 then does not exist! Then wait for BSY to clear and RDQ to set.
read data -> 512 bytes
See above for the interesting bytes from this.

#7 - 06/11/2018 09:09 PM - foft

What is used in set features?

0xef set features, then set feature 1 + lba mode?

Think this can probably be ignored.