EclaireXL - Feature #15

Implement programmable PLL

05/11/2017 09:41 PM - foft

Status:	New	**Start date:**	05/11/2017
Priority:	Normal	**Due date:**	
Assignee:		**% Done:**	0%
Category:		**Estimated time:**	0:00 hour
Target version:			

Description

See if the programmable PLL works. This will allow us to support different/custom VGA modes, once we have EDID/DDC working. For now I just want to find out if its alive.

History

#1 - 05/11/2017 09:42 PM - foft

- File Si5351-B.pdf added

Attaching PLL chip datasheet

#2 - 02/04/2018 09:22 PM - foft

- File Si5351A-RevB-Registers.h added

Attached header file for programming clk0->10MHz and clk1->30MHz.

These are generated with clock builder pro, downloaded from ic vendor web site.

#3 - 02/04/2018 09:23 PM - foft

- File AN619.pdf added

Attached the note on how to program manually (without clock builder help)

#4 - 02/04/2018 09:24 PM - admin

- Priority changed from Normal to Urgent

Going to power this up urgently before new boards made, to check hardware side is fine.

#5 - 02/04/2018 09:59 PM - foft

To do this I need to add i2c support to the ZPU. I'm out of ROM space without easy fixes. There is actually quite a lot space even on the EBA2, so adding 8K extra for now. Currently it was using bit 15 to decide rom/ram. I made it use 14 and 15 to choose ram. There is some hack I put in for the mist external sector buffer (it writes to ROM area!!) which might be broken by this.

#6 - 02/05/2018 09:58 PM - foft

Been adding i2c to the zpu. Mostly working I think, a few timing issues to solve.

#7 - 02/06/2018 08:49 PM - foft

- Priority changed from Urgent to Normal

OK, confirmed this chip is working. I programmed it over i2c and am now getting two different clocks output on CLK0 and CLK2 - 10MHz and 30MHz as I set up in the clk generator software.
Going to mark this back as normal priority since I now know the chip is connected ok and working.

#8 - 02/06/2018 09:15 PM - sadosp

foft wrote:

> OK, confirmed this chip is working. I programmed it over i2c and am now getting two different clocks output on CLK0 and CLK2 - 10MHz and 30MHz as I set up in the clk generator software.
> Going to mark this back as normal priority since I now know the chip is connected ok and working.

Congrats! ;-)

Files

Si5351-B.pdf	1.74 MB	05/11/2017	foft
Si5351A-RevB-Registers.h	9.33 KB	02/04/2018	foft
AN619.pdf	1.83 MB	02/04/2018	foft