

## EclaireXL - Feature #13

### 32x speed cpu without wait states

04/08/2017 08:08 PM - foft

<b>Status:</b>	New	<b>Start date:</b>	04/08/2017
<b>Priority:</b>	Normal	<b>Due date:</b>	
<b>Assignee:</b>	foft	<b>% Done:</b>	0%
<b>Category:</b>		<b>Estimated time:</b>	0:00 hour
<b>Target version:</b>			
<b>Description</b>			
The whole system is clocked at 32*original clock. However the 6502 turbo is limited to 16x due to the ram speed, since a block ram access cycle takes 2 cycles. Try to clock the block ram at 64* original clock as a quick win to get 32x turbo working.			

#### History

##### #1 - 04/08/2017 08:11 PM - foft

- Subject changed from High speed cpu to 32x speed cpu without wait states

##### #2 - 04/08/2017 08:25 PM - foft

- Tracker changed from Bug to Feature

##### #3 - 04/12/2017 10:07 PM - foft

- Status changed from New to In Progress

Trying simply feeding in the clock at twice the speed to see if it passes timing!

##### #4 - 04/26/2017 08:51 PM - foft

I have something working on the simulator - alone. Now need to plug it into the core proper to see if it works. Will probably need some clever timequest rules too, since the read/write deadlines are different now.

##### #5 - 05/04/2017 09:25 PM - foft

Nope, this is not going to be so simple... Massive timing violations.

##### #6 - 05/11/2017 08:38 PM - foft

So thinking about options...

Double the main clock speed and pipeline a bit

or

Output next address from antic and the cpu, so I can read the memory 1 cycle earlier - antic clearly knows what it will read, does the 6502 core?

or

Add a cache?!

##### #7 - 05/16/2017 09:24 PM - foft

I enabled 32x mode in the core and sorted out single cycle writes from the block ram for now. Hardly any difference in sysinfo but good to see at least some difference.

##### #8 - 05/30/2017 06:59 PM - foft

- Assignee set to foft

##### #9 - 05/31/2017 06:57 PM - foft

- Status changed from In Progress to New